Spartan-6 Family FPGAs

SPARTAN 6

		Spartan-6 LX FPGAs Optimized for Lowest Cost Logic, DSP, and Memory (1.2 Volt, 1.0 Volt)								Spartan-6 LXT FPGAs Optimized for Low Cost Logic, DSP, and Memory with High Speed Serial Connectivity (1.2 Volt)				
	Part Number	XC6SLX4	XC6SLX9	XC6SLX16	XC6SLX25	XC6SLX45	XC6SLX75	XC6SLX100	XC6SLX150	XC6SLX25T	XC6SLX45T	XC6SLX75T	XC6SLX100T	XC6SLX150T
Logic Resources	Slices [1]	600	1,430	2,278	3,758	6,822	11,662	15,822	23,038	3,758	6,822	11,662	15,822	23,038
	Logic Cells [2]	3,840	9,152	14,579	24,051	43,661	74,637	101,261	147,443	24,051	43,661	74,637	101,261	147,443
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	184,304	30,064	54,576	93,296	126,576	184,304
Memory Resources	Maximum Distributed RAM (Kbits)	75	90	136	229	401	692	976	1,355	229	401	692	976	1,355
	Block RAM (18K bits each)	12	32	32	52	116	172	268	268	52	116	172	268	268
	Total Block RAM (Kbits) [3]	216	576	576	936	2,088	3,096	4,824	4,824	936	2,088	3,096	4,824	4,824
Clock Resources	Clock Manager Tiles (CMT) [4]	2	2	2	2	4	6	6	6	2	4	6	6	6
I/O Resources	Maximum Single-Ended Pins	120	200	232	266	358	400	480	570	250	296	320	490	530
	Maximum Differential Pairs	60	100	116	133	179	200	240	285	125	148	160	245	265
Embedded Hard IP Resources	DSP48A1 Slices [5]	8	16	32	38	58	132	180	180	38	58	132	180	180
	PCI Express® Endpoint Block	—	—	—	—	—	—	—	—	1	1	1	1	1
	Memory Controller Blocks	0	2	2	2	4	4	4	4	2	2	4	4	4
	GTP Low-Power Transceivers	—	—	—	—	—	—	—	—	2	4	8	8	8
Speed Grades	Commercial	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3	-2, -3
	Industrial	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-L1, -2	-2	-2	-2	-2	-2
Configuration	Configuration Memory (Mbits)	2.7	2.7	2.7	4.4	7.7	19.6	17.1	28.0	4.4	7.7	19.6	17.1	28.0
Package	Area	Maximum User I/O: SelectIO™ Interface Pins (GTP Transceivers) [7]												
Chip Scale Packages (CPG): Pb-Free wire-bond BGA (0.5 mm ball spacing)														
CPG196	8 x 8 mm	100	100	100										
TQFP Packages (TQG): Pb-free thin QFP (0.5 mm lead spacing)														
TQG144	20 x 20 mm	100	102											
Chip Scale Packages (CSG): Pb-free wire-bond chip scale BGA (0.8 mm ball spacing)														
CSG225	13 x 13 mm	120	160	160										
CSG324	15 x 15 mm		200	232	226	218				190 (2)	190 (4)			
CSG484	19 x 19 mm					310	310	320	330		290 (4)	290 (4)	290 (4)	290 (4)
FGA Packages (FTG): Pb and Pb-free wire-bond fine-pitch thin BGA (1.0 mm ball spacing)														
FT(G)256	17 x 17 mm		186	186	186									
FGA Packages (FGG): Pb and Pb-free wire-bond fine-pitch BGA (1.0 mm ball spacing)														
FG(G)484	23 x 23 mm				266	316	TBD	326	338	250 (2)	296 (4)	TBD	296 (4)	296 (4)
FG(G)676	27 x 27 mm					358	400	480	498			320 (8)	376 (8)	396 (8)
FG(G)900	31 x 31 mm								570				490 (8)	530 (8)

Notes:
1. Each Spartan-6 FPGA CLB contains four LUTs and eight flip-flops.
2. Spartan-6 FPGA logic cell ratings reflect the increased logic capacity offered by the new 6-input LUT architecture.
3. Block RAMS are fundamentally 18Kb in size. Each block can also be used as two independent 9Kb blocks.
4. Each CMT contains two DCMs and one PLL.
5. Each DSP48A1 slice contains an 18x18 multiplier, an adder and an accumulator.
6. Preliminary product information, subject to change. Please contact your Xilinx representative for the latest information.
7. Due to the transceivers in the LXT devices, the LX pmouts are not compatible with the LX device pmouts.

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Spartan-3A, 3AN & 3A DSP FPGAs

		Extended Spartan-3A Family Optimized for Lowest Total Cost						
	Part Number	XC3S50A / AN	XC3S200A / AN	XC3S400A / AN	XC3S700A / AN	XC3S1400A / AN	XC3SD1800A	XC3SD3400A
Logic Resources	System Gates (1)	50K	200K	400K	700K	1400K	1800K	3400K
	Slices (2)	704	1,792	3,584	5,888	11,264	16,640	23,872
	Logic Cells	1,584	4,032	8,064	13,248	25,344	37,440	53,712
	CLB Flip-Flops	1,408	3,584	7,168	11,776	22,528	33,280	47,744
Memory Resources	Maximum Distributed RAM (Kbits)	11	28	56	92	176	260	373
	Block RAM Blocks (18k bits each)	3	16	20	20	32	84	126
	Total Block RAM (Kbits)	54	288	360	360	576	1,512	2,268
Non-Volatile Capability	Single Chip Option	Yes	Yes	Yes	Yes	Yes	No	No
	User Flash (Kbits) (3)	– / 627	– / 3,054	– / 2,380	– / 5,779	– / 12,251	—	—
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	8	8	8	8
I/O Resources	Maximum Single Ended I/Os	144 / 108	248 / 195	311	372	502	519	469
	Maximum Differential I/O Pairs	64 / 50	112 / 90	142	165	227	227	213
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, PCI-X 3.3V, SSTL3 Class I, SSTL3 Class II, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, SSTL18 Class II, Bus LVDS, LVDS25 & 33, LVPECL25 & 33, Mini-LVDS25 & 33, RSDS25 & 33, TMDS33, PPDS25 & 33						
Embedded Hard IP Resources	Multipliers/DSP48A Blocks	3	16	20	20	32	84 (4)	126 (4)
	Device DNA Security	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Speed Grades	Commercial	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial	-4	-4	-4	-4	-4	-4, -4L (5)	-4,-4L (5)
Configuration	Configuration Memory Bits (Kbits)	0.4	1.2	1.9	2.7	4.8	8.2	11.7
Package (6)	**Size**	**Maximum User I/Os**						
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)								
VQ100	16 x 16 mm	68 / – (7)	68 / – (7)					
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)								
TQ144	22 x 22 mm	108 / 108						
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)								
FT256	17 x 17 mm	144 / – (7)	195 / 195	195 / – (7)	161 / – (7)	161 / – (7)		
Chip Scale Packages (CS): wire-bond chip-scale BGA (0.8 mm ball spacing)								
CS484	19 x 19 mm						309 (5)	309 (5)
FGA Packages (FG): wire-bond fine-pitch BGA (1.0 mm ball spacing)								
FG320	19 x 19 mm		248 / – (7)	251 / – (7)				
FG400	21 x 21 mm			311 / 311	311 / – (7)			
FG484	23 x 23 mm				372 / 372	375 / – (7)		
FG676	27 x 27 mm					502 / 502	519	469

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic 3. Spartan-3AN User Flash is the space left in the on-chip Flash after a portion is used to store configuration bitstream 4. Integrated in the DSP48A slices (Advanced Multiply Accumulate element) 5. The L low-power option is exclusively available in CS(G)484 package and Industrial temperature range 6. All products available Pb-free and RoHS-Compliant, check datasheet for Pb package availability 7. Package not available in non-volatile Spartan-3AN family

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Spartan-3 & 3E FPGAs

		Spartan-3 FPGAs Optimized for High Density and High I/O Designs								Spartan-3E FPGAs Logic Optimized				
	Part Number	XC3S50	XC3S200	XC3S400	XC3S1000	XC3S1500	XC3S2000	XC3S4000	XC3S5000	XC3S100E	XC3S250E	XC3S500E	XC3S1200E	XC3S1600E
Logic Resources	System Gates [1]	50K	200K	400K	1000K	1500K	2000K	4000K	5000K	100K	250K	500K	1200K	1600K
	Slices [2]	768	1,920	3,584	7,680	13,312	20,480	27,648	33,280	960	2,448	4,656	8,672	14,752
	Logic Cells	1,728	4,320	8,064	17,280	29,952	46,080	62,208	74,880	2,160	5,508	10,476	19,512	33,192
	CLB Flip-Flops	1,536	3,840	7,168	15,360	26,624	40,960	55,296	66,560	1,920	4,896	9,312	17,344	29,504
Memory Resources	Maximum Distributed RAM (Kbits)	12	30	56	120	208	320	432	520	15	38	73	136	231
	Block RAM Blocks (18k bits each)	4	12	16	24	32	40	96	104	4	12	20	28	36
	Total Block RAM (Kbits)	72	216	288	432	576	720	1,728	1,872	72	216	360	504	648
Clock Resources	Digital Clock Managers (DCMs)	2	4	4	4	4	4	4	4	2	4	4	8	8
I/O Resources	Maximum Single Ended I/Os	124	173	264	391	487	565	633	633	108	172	232	304	376
	Maximum Differential I/O Pairs	56	76	116	175	221	270	300	300	40	68	92	124	156
	I/O Standards Supported	LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, GTL, GTL+, HSTL15 Class I, HSTL15 Class III, HSTL18 Class I, HSTL18 Class II, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, SSTL2 Class I, SSTL2 Class II, SSTL18 Class I, Bus LVDS, LDT (ULVDS), LVDS_ext, LVDS25 & 33, LVPECL25, RSDS25								LVTTL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVCMOS12, HSTL18 Class I, HSTL18 Class III, PCI 3.3V 32/64bit 33MHz, PCI 3.3V 64bit/66MHz, PCI-X 3.3V, SSTL2 Class I, SSTL18 Class I, Bus LVDS, LVDS25, LVPECL25, Mini-LVDS25, RSDS25				
Embedded Hard IP Resources	Dedicated Multipliers	4	12	16	24	32	40	96	104	4	12	20	28	36
Speed Grades	Commercial	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5	-4, -5
	Industrial	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4	-4
Configuration	Configuration Memory Bits (Mbits)	0.4	1.0	1.7	3.2	5.2	7.7	11.3	13.3	0.6	1.4	2.3	3.8	6.0
Package [3]	Area	Maximum User I/Os												
VQFP Packages (VQ): very thin QFP (0.5 mm lead spacing)														
VQ100	16 x 16 mm	63	63							66	66	66[4]		
Chip Scale Packages (CP): wire-bond chip-scale BGA (0.5 mm ball spacing)														
CP132	8 x 8 mm	89								83	92	92		
TQFP Packages (TQ): thin QFP (0.5 mm lead spacing)														
TQ144	22 x 22 mm	97	97	97						108	108			
PQFP Packages (PQ): wire-bond plastic QFP (0.5 mm lead spacing)														
PQ208	30.6 x 30.6 mm	124	141	141							158	158		
FGA Packages (FT): wire-bond fine-pitch thin BGA (1.0 mm ball spacing)														
FT256	17 x 17 mm		173	173	173						172	190	190	
FGA Packages (FG): wire-bond chip-scale BGA (1.0 mm ball spacing)														
FG320	19 x 19 mm			221	221	221						232	250	250
FG400	21 x 21 mm												304	304
FG456	23 x 23 mm			264	333	333	333							
FG484	23 x 23 mm													376
FG676	27 x 27 mm				391	487	489	489	489					
FG900	31 x 31 mm						565	633	633					

Notes: 1. System Gates include 20%-30% of CLBs used as RAMs. 2. Each slice comprises two 4-input logic function generators (LUTs), two storage elements, wide-function multiplexers, and carry logic.
3. All products available Pb-free and RoHS-Compliant. 4. Available only in VQG100 package. VQG100 and VQ100 have identical pinouts.

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